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ISSN: 2277-9655
[Pandey * *et al.*, 6(9): September, 2017] Impact Factor: 4.116
IC™ Value: 3.00 CODEN: IJESS7

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

A VLSI IMPLEMENTATION FOR HIGH SPEED AND HIGH SENSITIVE FINGERPRINT SENSOR USING CHARGE ACQUISITION PRINCIPLE

Kumudlata Bhaskar[1], Kamal Prakash Pandey[2*] & Chandrabhan[3]
[1] M.Tech Scholar SIET Allahabad
[*2&3]Associate Professor, SIET Allahabad

DOI: 10.5281/zenodo.995991

ABSTRACT

In this proposed work, we have implemented 80X64 Array high sensitive fingerprint sensor with capacitive charge acquisition principle. It used charge transfer acquisition principle for sensing the change in capacitance. The electrode capacitance is charged to the stable reference voltage. The charge is then transferred to a known capacitor referred to as the sampling capacitor (CS). This sequence is repeated until the voltage on the CS capacitor reaches an internal reference voltage. The number of transfers required to reach the threshold depends on the size of the electrode capacitance and represents its value. The ADC resolution has been increased and thus to ensure stable operations, number of transfers needed to reach the threshold is adjusted by IIR Filter which compensates for environmental changes such as temperature, power supply, moisture, and surrounding conductive objects. The operation is validated by TSPICE for one-pixel and RTL simulation by Xilinx ISE including logic synthesis for the full chip design on condition of 0.18µm typical CMOS process and 1.8V power.

KEYWORDS: Capacitive touch sense, Fingerprint sensor array, sampling capacitor, TSPICE, IIR Filter

I. INTRODUCTION

Capacitive sensing interfaces are more and more used in a wide range of applications. The interface is based on surface sensors that are made of small copper foils. The sensor acts as a capacitor that is alternatively charged and discharged. The capacitor value depends on the presence of the user finger as well as the sensor design The surface charge transfer acquisition is a proven, robust and efficient way to measure a capacitance. It uses a minimum number of external components to operate with a single ended electrode type. This acquisition is designed around an analog I/O group which is composed of four GPIOs. Several analog I/O groups are available to allow the acquisition of several capacitive sensing channels simultaneously and to support a larger number of capacitive sensing channels.

Within a same analog I/O group, the acquisition of the capacitive sensing channels is sequential. One of the GPIOs is dedicated to the sampling capacitor (CS). Only one sampling capacitor I/O per analog I/O group must be enabled at a time. The remaining GPIOs are dedicated to the electrodes and are commonly called channels. For some specific needs (such as proximity detection), it is possible to simultaneously enable more than one channel per analog I/O group. The surface charge transfer acquisition principle consists of charging an electrode capacitance (CX) and transferring a part of the accumulated charge into a sampling capacitor (CS). This sequence is repeated until the voltage across CS reaches a given threshold (VIH in our case). The number of charge transfers required to reach the threshold is a direct representation of the size of the electrode capacitance. When the electrode is “touched”, the charge stored on the electrode is higher and the number of cycles needed to charge the sampling capacitor decreases.

Traditional automatic personal identifications, such as personal identification numbers (PINs), identification cards, and keys are no longer satisfactory for recent security requirements. Biometrics, the automatic identification of a person on the basis of certain physiological or behavioral characteristics, is one of the technologies that can be applied to the fulfillment of security requirements, because each individual has unique characteristics that are relatively constant over time [1].

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The fingerprint is known to be the most representative bio-metric for authentication of individual persons. Some research organizations have published papers on semiconductor-based sensing schemes and demonstrated the possibility of a single-chip solution. A capacitive fingerprint sensor uses a capacitive sensor array to detect fingerprints. The name 'capacitive' comes from the fact that the finger skin and the sensor electrode produce a capacitor whose capacitance is determined by the distance from the chip surface to the finger skin. The finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode as shown in Figure 1.

One of the most important performances of a capacitive sensor is the sensitivity capability since the detected capacitance is very small of the order of femto-farads. A charge-sharing sensing scheme has a high sensitivity and a simple circuit structure for the restricted pixel area below a sensor plate. Some papers on charge-sharing sensing scheme have been published [2, 3 4]. The paper [2] proposed the removing of parasitic capacitance using unit-gain buffer, and paper [3, 4, 5, 6] proposed the improvement of difference between a ridge and valley detection voltage using a feedback resistor. Although these methods are useful in dramatic performance improvement, a static current can exist on a sensing enable phase in these circuits because of a unit-gain buffer and feedback resistor

II. FRINGERPRINT SENSING SCHEME

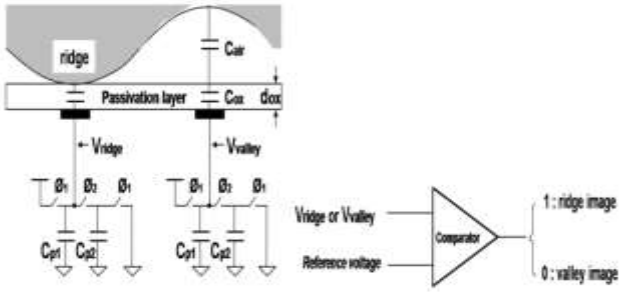

Fig.1. Model of capacitive fingerprint sensing scheme

Capacitive sensing devices may suffer from more parasitic components in their touch sensitivity and performance. A capacitive sensor based on charge transfer circuit has also been introduced [5-7]. This paper adopts charge transfer circuit based on the active output voltage feedback integrator. Figure 1 shows the charge transfer integrator based on active output voltage feedback circuit [4]. The finger is simply modeled with a series resistor and a capacitor formed between the finger and a chip surface, Cf. A parasitic capacitor between the sensor plate and isolation metal is represented as Cp1. The sensor plate is isolated by a metal to prevent the noise from the circuit under the sensor plate as shown in figure 2, which forms a parasitic capacitance between the sensor top metal plate and under metal. Since Cp1 is relatively large compared to Cf, it should be removed. Some methods for eliminating Cp1 have been developed [2]. To remove simply Cp1, the output is applied to the bottom node of Cp1 to maintain the same potential of the both nodes of Cp1, which maximizes the sensitivity of the fingerprint sensor.

III.

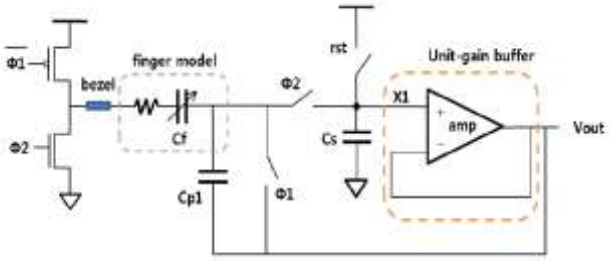

Fig.2. One pixel of Charge acquisition circuit

This paper proposes an efficient hardware design for processing of fingerprint identification through charge acquisition principles. A thinning algorithm changes a binary fingerprint image to one pixel width. Even though a thinning operation is very simple, it occupies very much cycle of microprocessor system. Hardware processing

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is more effective than software algorithm in speed, because a thinning algorithm is iteration of simple instructions. The cycle distribution of each algorithm step is analyzed in FPGA and also performs the RTL implementation of charge acquisition algorithm

IV. CAPACITIVE FINGER PRINT SENSOR

Fingerprint sensor depending on capacitive sensing scheme is generally constructed as Fig. 1. In microscopic scale, the surface on the finger may have deeper part like valley or more elevated like ridge. In standard CMOS process the top metal can be exploited as the fingerprint sensor plate where the area of the sensor plate is denoted as A. As the fingertip surface approaching the sensor plate, capacitance can be induced according to two factors: dielectric constant (εx) and the distance between the surface and the sensor plate (dx).

V.

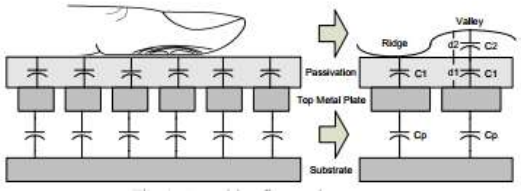

Fig.3 Capacitive fingerprint sensor module

While the valley part will produce a much smaller capacitanceof C2 (C2 = Aε2/d2) in series with C1. According to the parameters of standard CMOS process and required resolution, a pixel size of about 50μm × 50μm to achieve 500 pixels per inch well suitable for fingerprint image acquisition, hence a reasonable estimation on the induced capacitance is ranged from 0 to 60 fF.

VI. RESULTS & DISCUSSSION

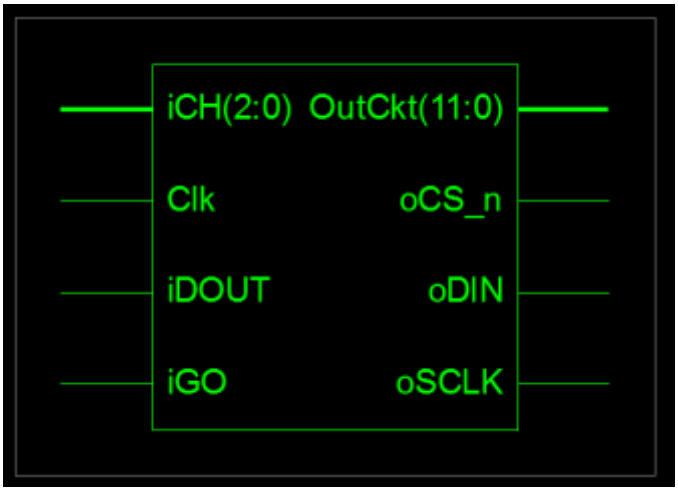

Fig.4 Block structure of the ADC Module

Fig.4 presents the block structure of the ADC Module showing its all inputs and outputs. Here, the data converter input pins include 3-bit Channel select pin (iCH), the conversion clock input pin (clk), Data conversion in (iDOUT), and start conversion input pin (iGO).

Here, ADC Output includes 12-bit output pins, Chip select for fingerprint module and output clocks

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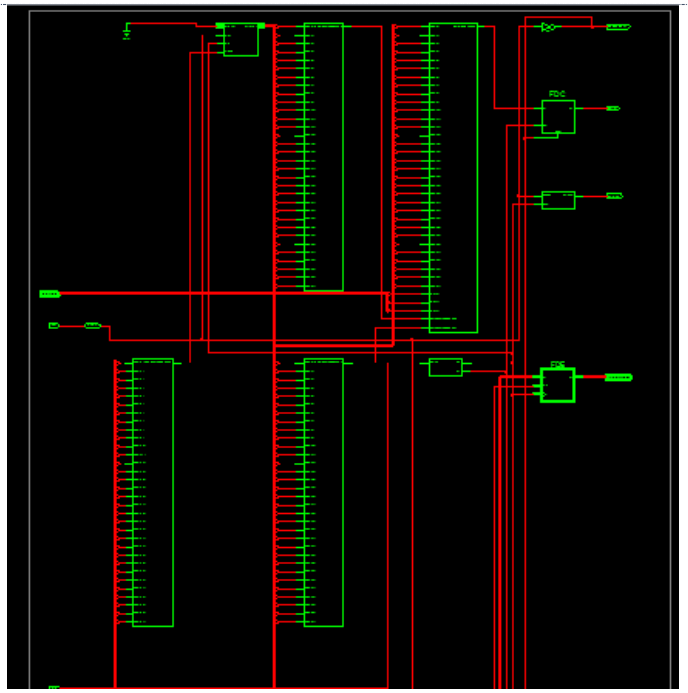

Fig.5 RTL structure of ADC data register structure

VII.

Here, the detailed RTL structure ADC module has been presented. The ADC data register has been presented here. The chip structures are been presented here.

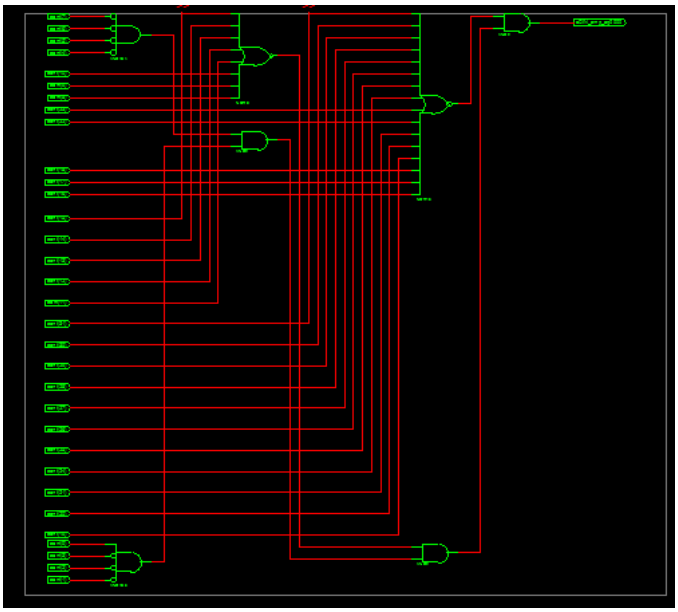

Fig.6 Data conversion functional block

VIII.

Here, In fig.6 the RTL structure of the functional unit of the converter design has been presented. The unit block consists of the converter lines, the internal data lines and gates for final conversion, buffer for final data storage.

Similarly, in Fig.7 the RTL structure of overall functional system has been presented. The structure has been presented over for the final structural unit display for the fingerprint sense module

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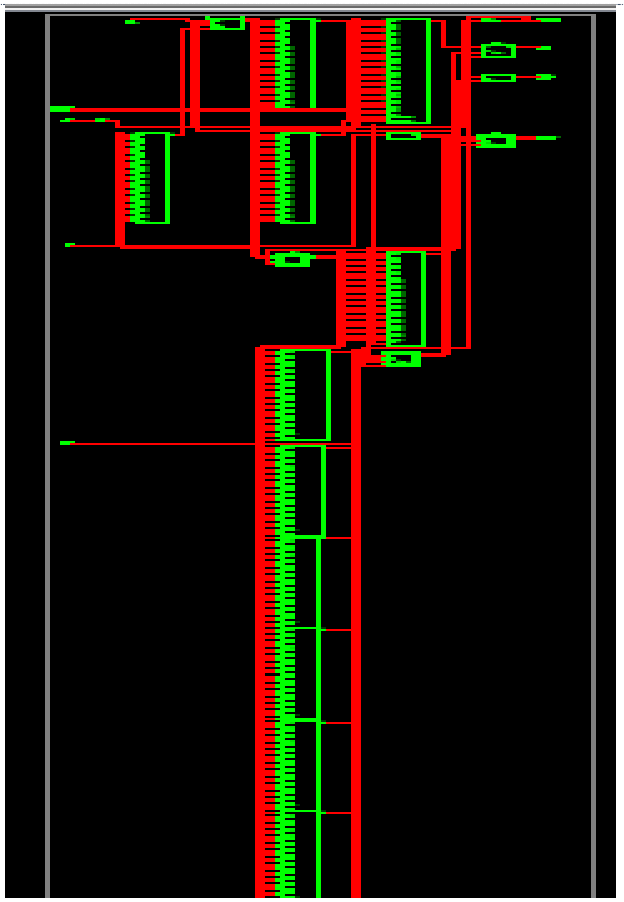

Fig.7 Magnified view of the final structure of the fingerprint module

Fig.7 presents the magnified view of the fingerprint module showing all the features of the final structure of the module. All the data buses of the internal module has been presented. Thus, the hardware design has been presented

IX. CONCLUSION

Thus, in our proposed work we have presented the hardware structure of the proposed system architecture. The SAR based Flash – ADC design has been presented and the RTL view structure of the entire module has been presented. All the validation has been done by 100MHz clock and 12-bit ADC.

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CITE AN ARTICLE

Bhaskar, K., Pandey, K. P., & C. (2017). A VLSI IMPLEMENTATION FOR HIGH SPEED AND HIGH SENSITIVE FINGERPRINT SENSOR USING CHARGE ACQUISITION PRINCIPLE. *INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY*, *6*(9), 555-560.